

Design Considerations for a Feedback System to control Self-Bunching in Storage Rings

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Overview

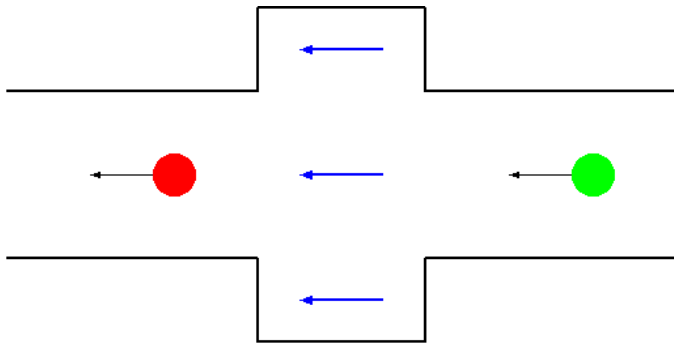
- The Problem ... and its causes
- Simulating the Problem
- Simulating the Solution
- Feedback Imperfections
- Conclusions

The Problem ...

- Self-Bunching
 - Normally run coasting beam with heavy ions because cooling works better and the detector event rate is more evenly distributed.
 - All of a sudden the beam starts to bunch.
 - Visible on oscilloscope with BPM sum signal
 - Zero-Span at revolution harmonic on spectrum analyzer
- Sometimes accompanied by particle loss
- reduces current → bad
- increases background → bad

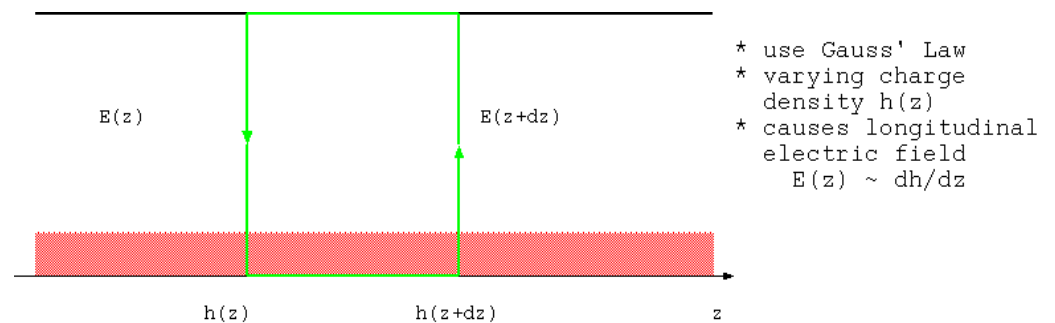
...and its causes

- **Impedances:** particles at different positions in the beam talk to each other
- **Geometric:** discontinuities of the vacuum chamber



- **Leading** particle deposits energy in resonator-like structure that **trailing** particle sees.
- Wake field: $W(z)$
- Energy loss: $U(z)$

- **Space Charge:** (A. Hoffmann, CERN 77-13)



- Electric field is proportional to derivative of line charge density.
- In a circular accelerator impedances lead to a
particle 1 \rightarrow particle 2 \rightarrow particle 1
loop which can become unstable.
- Fluctuations can be enhanced and pile up
 \rightarrow Self-Bunching

Simulating the Problem 1

- Multiparticle simulation with typically 10000 particles.

- Unperturbed dynamics:

$$\varphi_{n+1} = \varphi_n + \eta(dp/p)_n \quad (dp/p)_n = (dp/p)_{n+1}$$

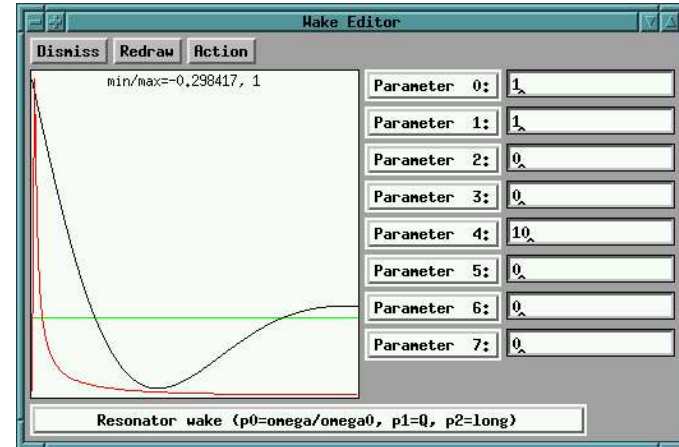
- Wake fields

- 256 longitudinal bins N_i
- Wakefield is given as array[256]

- Influence of wakes on the dynamics

$$\Delta \left(\frac{dp}{p} \right)_{\text{bin } i} \propto \sum_{\text{all previous bins, called } j} W((i-j) \bmod 256) N_j$$

- Resonator Wake with $Q=1$



$$Z(\omega) = \frac{R_s}{1 + iQ(\omega/\omega_r - \omega_r/\omega)}$$

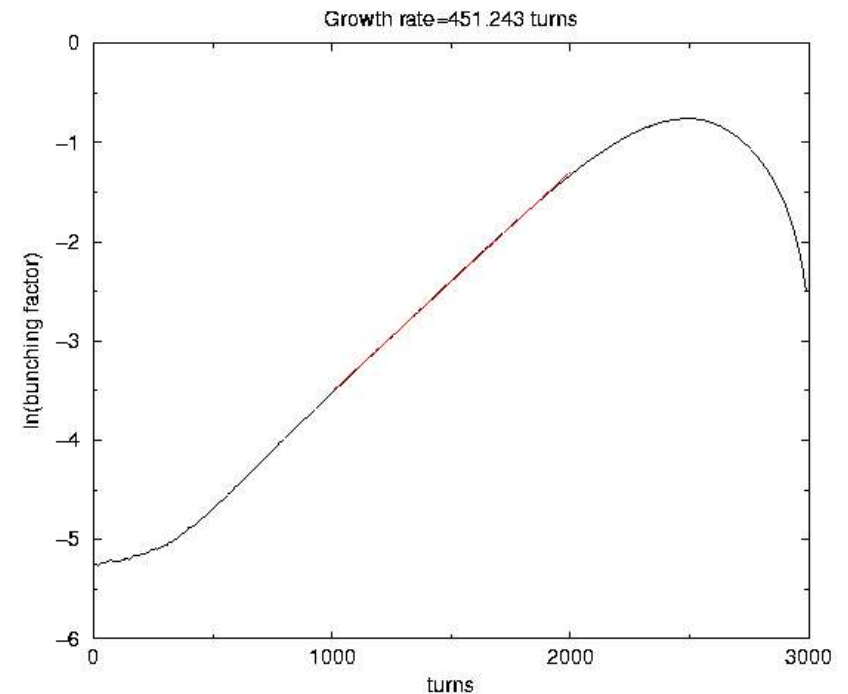
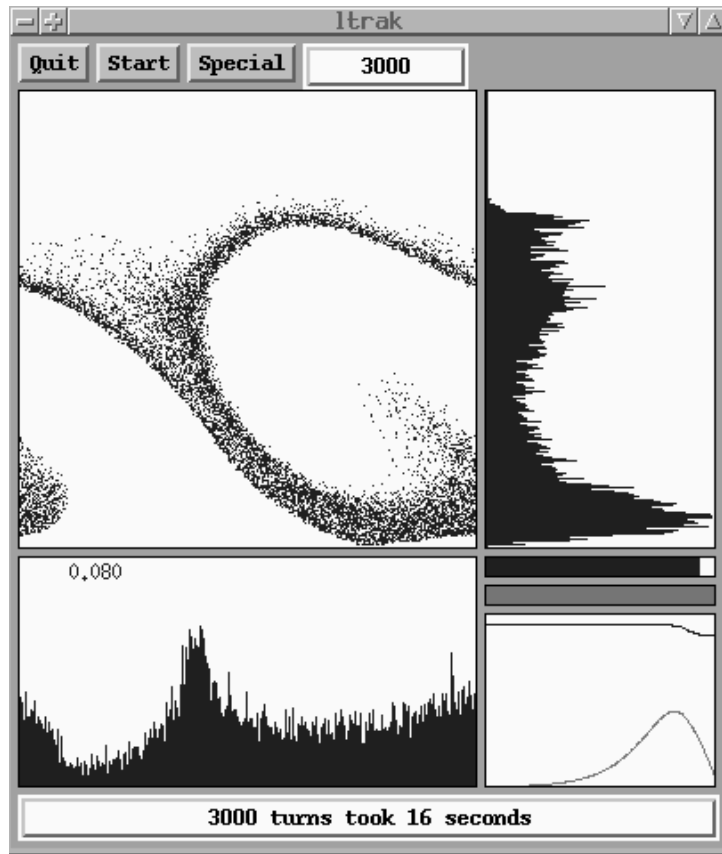
$$W(\tau) = e^{-C\tau} [A \cos(D\tau) - B \sin(D\tau)]$$

- Space charge:

- derivative of delta function
- capacitive wake
- high-pass filter, adds noise

Simulating the Problem 2

- Phase space, projections, bunching factor and current.
- Use growth rate of bunching factor as figure of merit.



Simulating the Solution 1

- Observation: Similarity between wake and finite impulse response (FIR) filter

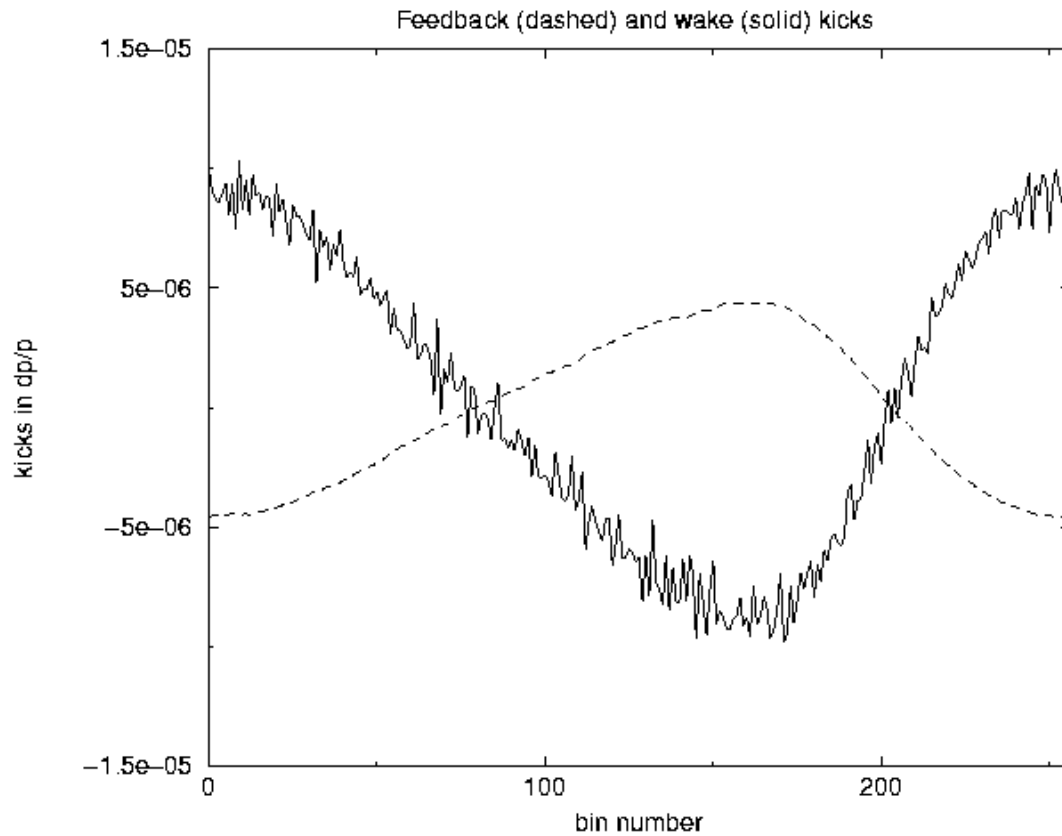
Input signal \rightarrow Filter coefficients \rightarrow Output Signal

Instantaneous beam current \rightarrow wake potential \rightarrow longitudinal electric field

- FIR filter coefficients == array[256]
- Record BPM sum signal
 - pass through FIR filter
 - record in (ring) buffer with length 8×256
 - pick kicks from the ring buffer with adjustable delay and apply to beam with negative sign
- Try different FIR filter coefficients
 - low pass NO!
 - high pass NO!
 - use wake function OK! (maybe not so surprising...)

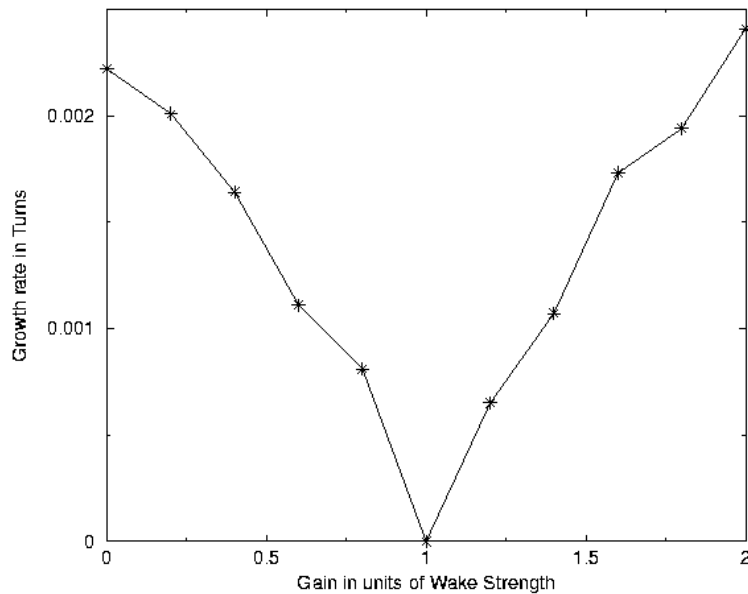
Simulating the Solution 2

- Simulate with half strength feedback

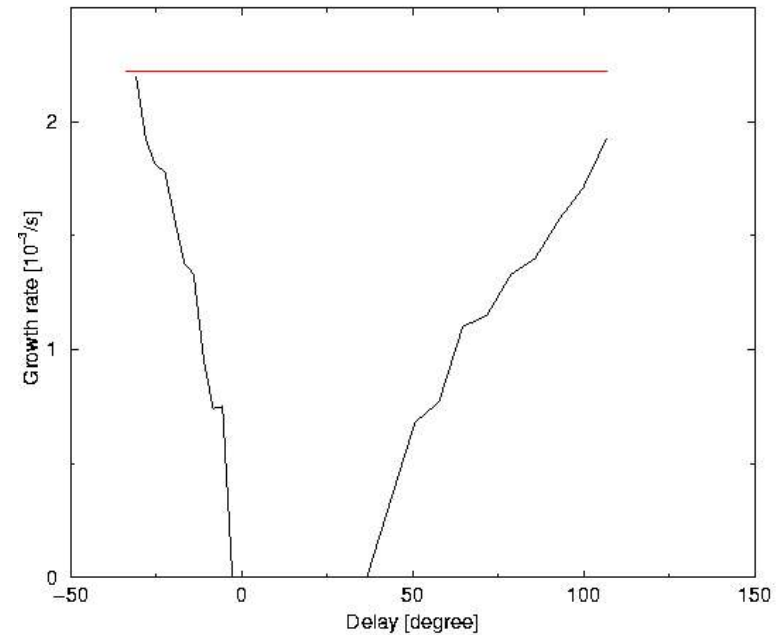


Feedback Imperfections

- Mis-adjustment of feedback gain.

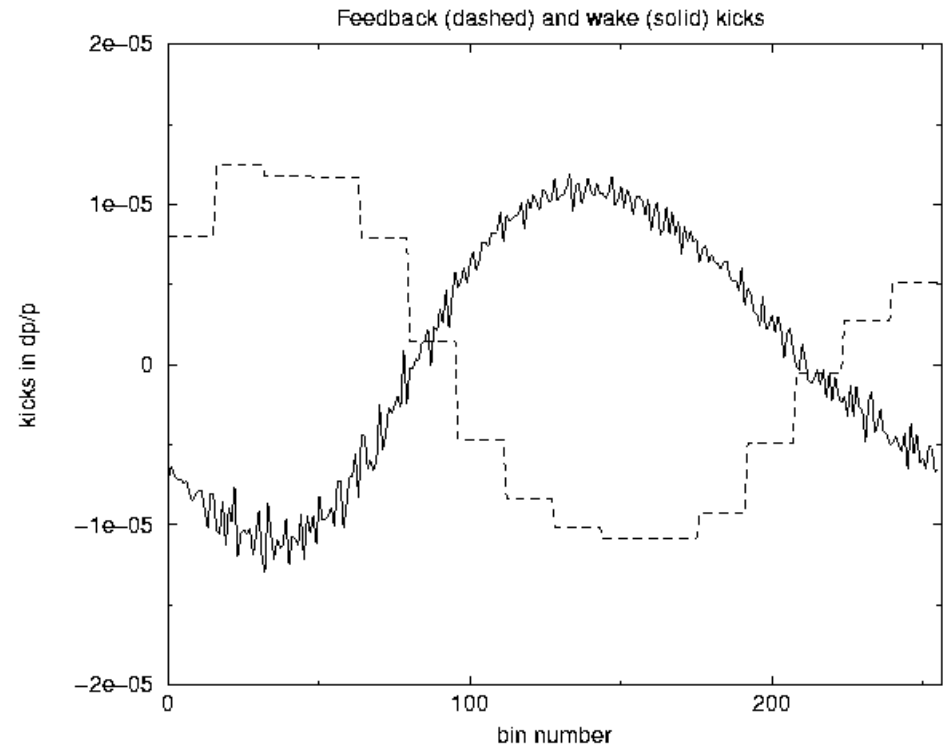


- Vary the time delay
- 40° window OK
- Kicking earlier is better



Feedback Imperfections

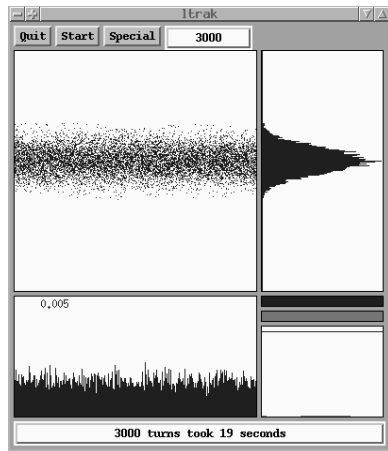
- Digitize Filter Coefficients
 - Need to correct DC offset.
 - 3 bit is sufficient.
 - 6 to 8-bit ADC makes matching of dynamic range easier.
- Saturation of amplifiers: can contain small fluctuations.
- Varying Q in FIR-wake is uncritical.



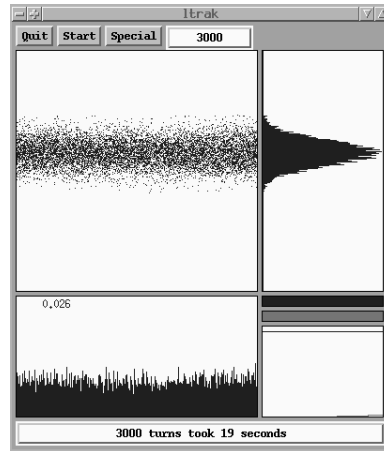
Sampling at lower Rates

(pick a kick from ring-buffer and hold constant for several consecutive slices)

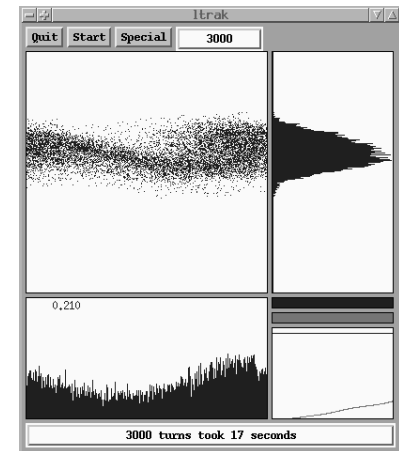
128
MHz



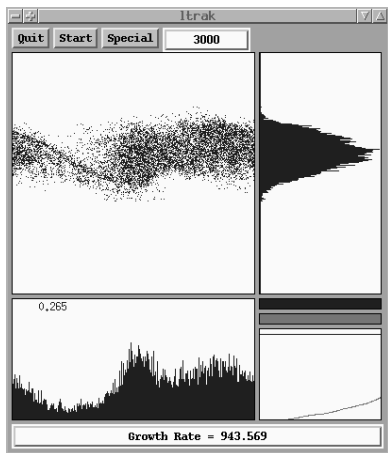
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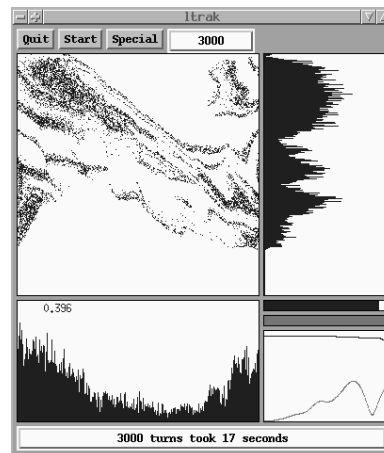
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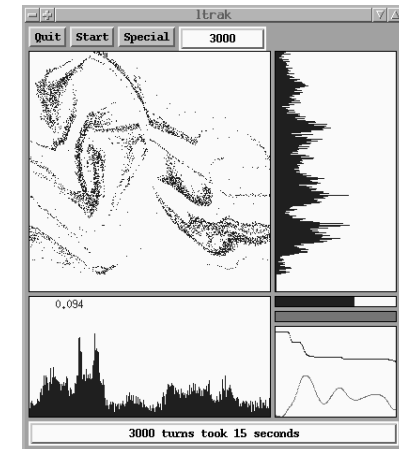
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8

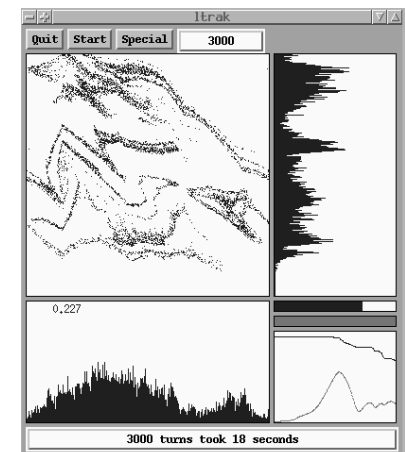
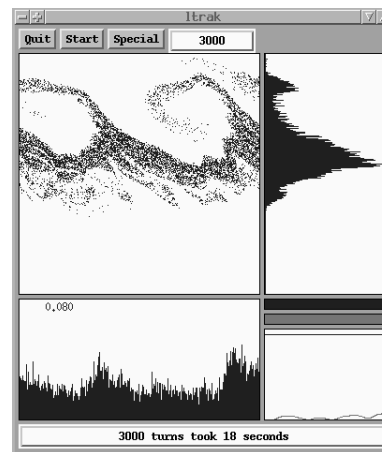
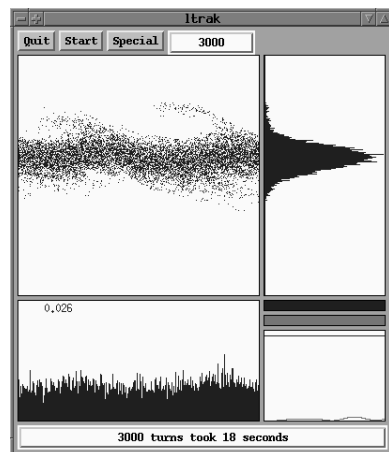
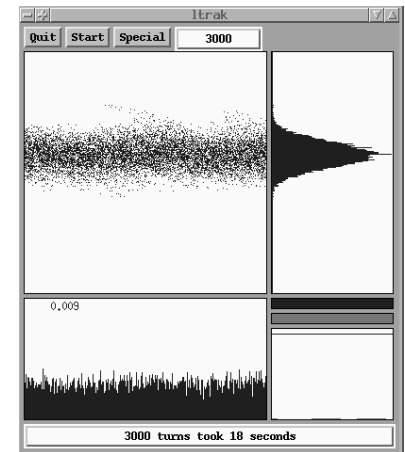
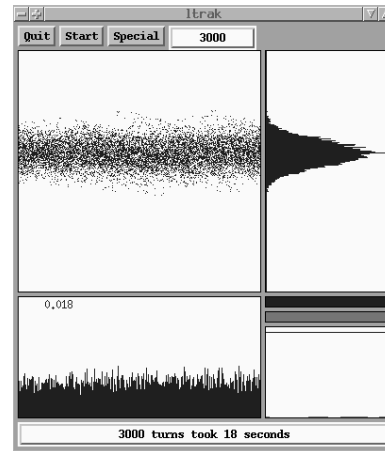
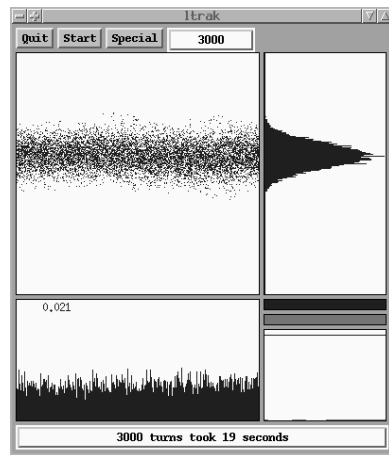


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Lower Rates plus Time Delay

(same as previous slide, but increase phase by 35° , i.e. kick a little earlier)



Conclusions

- **Need:**

- 30 x rev sample rate
- 60 filter taps
- 6 to 8 bit accuracy
- several 100 V

- **Implementation:**

- FPGA with distributed arithmetic
- Demo board with ADC+FPGA+DAC commercially available (few k\$)

- **Problems:**

- real wake is unknown, need to play with filter coefficients (easy on FPGA)
- Transfer function of amplifier and kicker
- Pickups are often AC-coupled, need DC signal which could be added synthetically.



1. Product Features

- On-board Xilinx Virtex-II FPGA
- Various FPGA device packages, sizes and speed grade options available
- Two independent analogue capture channels
- 2x 14-Bit ADC Resolution, up to 105MSPS per channel sampling rate
- Two independent channels to extract analogue data
- 2x 14-Bit DAC Resolution, 160MSPS per channel sampling rate
- Up-to 8MB of ZBT SRAM memory, in two independent banks.
- Nallatech ZBT SRAM interfacing IP Core available
- Multiple Clocking Options: Internal & External
- Example designs and source code included



2. Overview

The BenADDA provides high-speed digital-to-analogue and analogue-to-digital conversion. As part of the scalable DIME-II family, the BenADDA can be easily integrated into systems, through the range of available DIME-II motherboards and associated software/firmware. At the heart of the BenADDA is the on-board Xilinx® Virtex™-II FPGA, which provides a powerful data processing resource. Various FPGA devices, ranging from XC2V250 up-to XC2V6000, with a choice of speed grades are available. The BenADDA also offers the option of on-board ZBT SRAM memory, using 1MByte devices.

2.1.1 Digital to Analogue Conversion

The BenADDA offers flexible, high-speed, high-resolution data conversion for both baseband and direct IF applications. Two Analog Devices AD9772A DACs with a maximum reconstruction bandwidth of 67.5MHz at 160MSPS are directly controlled by the on-board FPGA, allowing users maximum operating flexibility.

2.1.2 Analogue to Digital Conversion

The BenADDA features two Analog Devices AD6644 ADCs. The AD6644 is a high-performance, monolithic 14-Bit analogue-to-digital converter with a sampling speed of 65MSPS. The sampled data can be processed directly by the on-board FPGA.

Demo Board

- XILINX Virtex-II FPGA
- 2x 14 bit ADC at 105 Ms
- 2x 14 bit DAC at 160 Ms